Cross-Switched Multilevel Inverter using Novel Switched Capacitor Converters

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***Abstract*—In this paper, a novel structure of switched capacitor converter (SCC) is proposed. First, the basic unit of the proposed SCC is presented. After that, a generalized structure of the proposed SCC is discussed. The presented SCC uses one dc source, several switches, diodes and capacitors to produce multistep dc boosted output voltage. The capacitors in the SCC can be charged in trinary asymmetrical pattern. A detailed comparative study between proposed and other recently developed SCC structures is presented. It is shown that the proposed SCC can produce an output voltage level with lower total standing voltage (*TSV*) and lower maximum switch stress voltage as compared to most of suggested SCC structures. Further, a Switched Capacitor Multilevel Inverter (SCMLI) based on Cross-Switched Multilevel Inverter (CS-MLI) has been developed and analyzed for symmetric and asymmetric dc source configurations. For fair comparison with the existing SCMLI structures, the overall cost of the structures are compared based on a cost function (*CF*). The proposed SCMLI provides lower cost function/output voltage level (CF/N_L) in comparison with most of the other SCMLI structures for both symmetric and asymmetric dc source configurations. Extensive experimental studies validate the operation and performance of the proposed SCMLI structure.**

***Index Terms*—Boosting, Multilevel Inverter, Switched Capacitor, Total Standing Voltage, Voltage Balance**

I. INTRODUCTION

IN recent years, to meet the challenges of producing high quality output voltage waveform, the demand of multilevel inverters (MLIs) have increased significantly in different fields of applications such as motor drives, electric vehicles, distributed generation systems, renewable energy conversion systems, FACTs, UPS systems, induction heating systems etc **[1-4]**. In a general sense, MLIs are able to synthesize stepped output voltage waveform with a better quality of harmonic spectrum using switches, diodes, capacitors and dc voltage sources. MLIs provide lower voltage stress on switching devices, lower electromagnetic interference (EMI) on output waveforms, they require smaller output filters, they have capability of handling high power levels as compared to the classical two-level inverters. Conventionally, MLIs are classified into three categories: neutral point clamp (NPC), flying capacitors (FC) and cascaded H-bridge (CHB). Although these conventional MLIs have proven their unique features and have become viable conversion topologies in different industrial applications, these topologies suffer from the requirement of large number of components to produce output voltage with higher levels. In addition, the capacitor voltage unbalancing problem and self-voltage boosting inabilities are other major limitations of conventional MLIs [**5**].

To overcome the limitation of large component requirements in conventional MLIs, different innovative "Reduced Device Count" (RDC) MLI topologies have been proposed in the literature [**6-9**]. But these RDCMLIs do not possess the self-voltage boosting capability to achieve a desired output voltage from lower input voltage supplies such as photovoltaic cells.

To meet the challenges of capacitor voltage unbalance problem, auxiliary circuits or complex control algorithms have been introduced in the literature [**10-12**]. Further, to incorporate the self-voltage boosting capability to conventional MLIs, auxiliary circuits such as front-end boost converters or impedance networks are connected with the inverters[**13-14**]. It may be noted that these solution methodologies for solving the capacitor voltage unbalance problem or self-voltage boosting inabilities enhance the size, cost and complexity of overall conversion systems.

In recent years, switched capacitor multilevel inverters (SCMLIs) have become one of the popular solutions to above mentioned challenges of conventional MLIs due to their unique features. SCMLIs can produce near sinusoidal output voltage waveform using capacitors as alternate dc power supplies. In addition, capacitors help to boost the input voltages at the output terminals. Another one of the major advantages of SCMLIs is that they do not require any auxiliary circuits or complex algorithms to balance capacitor voltages. The concept of SCMLI was first proposed by O. C. Mak and A. Ioinovici by implementing a switched capacitor (SC) basic unit consisting of two switches, two diodes and one capacitor in 1998 **[15]**. In this paper, the authors proposed a 31 level SCMLI based on these SC basic units. However, the proposed structure required a large number of semiconductor devices and a relatively complex control algorithm to balance the capacitor voltages. The authors of **[16]** have proposed a SCMLI structure based on boost converter and an H-bridge circuit. The boost converter with switched capacitor can

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generate multilevel dc voltage and the H-bridge is used as polarity generation circuit at the load terminals. However, for achieving higher voltage levels, the topology requires significant number of capacitors, active switches and diodes. To reduce the capacitor requirement in **[16]**, the authors of **[17]** have proposed a SCMLI structure which can realize multiple voltage levels by utilizing the partial charging of capacitors. However, the topology requires significant number of switches to establish the concept of partial charging of the capacitors. Based on the SCMLI presented in **[15]** and the Marx inverter, a novel SCMLI structure has been proposed by the authors of **[18].** The presented structure in [**18**] is capable of synthesizing the different output voltage levels and can maintain the capacitor voltages at the desired values by switching the capacitors in series/parallel mode with respect to the input source. However, the topology requires an H-bridge circuit which enhances the total standing voltage (*TSV*) of the inverter structure. In addition, for enhancing the output voltage level, the requirement of semiconductor devices and capacitors increase significantly. A novel SC basic unit utilizing two switches, one diode and one capacitor has been proposed by the authors of **[19]**. Based on these SC basic units, two hybrid multilevel inverter structures have been presented in **[19]**. Both the presented structures require H-bridge circuits which enhances the *TSV* of the proposed inverters. A cascaded MLI based on SC basic unit as presented in [**19**] for high frequency ac distribution system has been presented by the authors of [**20**]. The presented structure in [**20**] has been analyzed for symmetric dc source configuration. Each SC basic unit is incorporated with an H-bridge circuit which enhances the *TSV* and component count of the circuit as the output voltage level increases. With a little modification of SC basic unit of [**19**-**20**], the authors of [**21**] have proposed a SCMLI which reduces the number of required switching devices. However, the topology requires an H-bridge circuit which enhances the *TSV* of the structure. A novel structure of switched capacitor converter (SCC) has been proposed by the authors of **[22]**. The proposed SCC can produce fixed dc to multilevel boosted dc voltage levels by charging and discharging the capacitors in binary asymmetrical pattern. Using these proposed SCCs, the authors of **[22]** have proposed a MLI structure. Further, the authors of **[23]** have presented a SCMLI structure based on the same SCC structure as presented in [**22**]. Both the MLI structures have been analyzed for asymmetric dc source configuration and have the ability to generate a great number of voltage levels using reduced number of switching devices. However, the SCC and the MLI structures of [**22**-**23**] suffer from the high voltage stress across the switching devices and diodes which significantly enhances the *TSV* of the structures. A step-up MLI structure with multiple number of simultaneously charging and discharging possibilities of capacitors has been proposed by the authors of [**24**]. However, the topology requires large number of bidirectional switches to increase the charging possibilities in the circuit and *TSV* of the structure significantly increases as the output voltage level increases. Based on developed H-bridge and the SC basic unit as proposed in [**19**-**20**], the authors of [**25**] have presented a high-step up MLI structure. The structure has been analyzed for symmetric and asymmetric dc source configuration. The structure sustains high *TSV* as the output voltage level enhances. A novel SCMLI structure with reduced switching devices has been presented by the authors of **[26]**. The basic unit of the structure is able to produce 9 output voltage levels using 1 dc source, 2 capacitors, 1 diode and 10 switches. Further, an extended general SCMLI structure has been developed and analyzed for symmetric and asymmetric dc source configurations. However, the structure sustains higher *TSV* as the output voltage level enhances.

One of the major limitations of SCMLI structure is the high stress voltage across the semiconductor devices when the boosting factor of the inverter increases. This drawback enhances the cost of the inverter structure significantly. Hence, for cost effective solution, the SCMLI structure should not suffer from higher device count and higher *TSV* of the structure. In this paper, the basic unit of a novel switched capacitor converter (SCC) is proposed first. After that, a general structure of the proposed SCC has been developed. A detailed operating principle, such as how it produces dc multilevel voltage from a single dc source has been presented. After that, the SCC structure is compared with recently published SCC structures with respect to different aspects. Further, a cross switched MLI (CS-MLI) structure has been developed based on the proposed SCCs. The SCMLI structure has been analyzed for symmetric and asymmetric dc source configurations. The selection procedure of switched capacitors has been explained next. A comparative study of proposed SCMLI with other SCMLIs is discussed. At last, the merits and effectiveness of proposed SCMLI is verified by extensive experimental studies.

II. Basic Unit of Proposed SCC

Fig. 1 shows the basic unit (BU) of proposed SCC circuit. It consists of one dc power supply V_{in}, two capacitor legs L1 and L11, and one charging leg CH1. L1 and L11 consist of two unidirectional power switches (S_1 and S_1' for L1 and S_2 and S_2' for L11) and a capacitor (C_1 for L1 and C_{11} for L11) as shown in Fig. 1. CH1 is formed by a power switch S_{1c} along with a series connected power diode D_1. The mid-points of L1 and L11 are connected to positive and negative terminals of V_{in} respectively. Further, L1 and L11 are connected in series by CH1. The switch S_{1c} of CH1 will be in on state only when the charging state of the capacitors (either C_1 or C_{11}) are initiated.

Fig. 2 presents the equivalent circuit and current flow paths for the proposed BU corresponding to the different voltage levels generated at its output terminals *A* and *O*. Further, the different switching and capacitor states for the BU are tabulated in Table I. Where '1' and '0' stand for on and off state of switches and C, D and NC indicate charging, discharging and not-connected state of capacitors respectively. Fig. 2(a) shows the equivalent circuit and the current flow path (in red line) when V_{AO} is equal to $+V_{in}$. This voltage level can be achieved by turning on the switches S_1' and S_{11}' and turning off the switches S_1 and S_{11} as shown in Table I. At this instant, C_1

and C_{11} are in NC state that means they are neither in charging nor in discharging state.

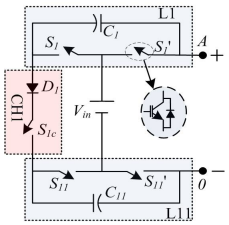

Fig.1. Basic unit of proposed SCC

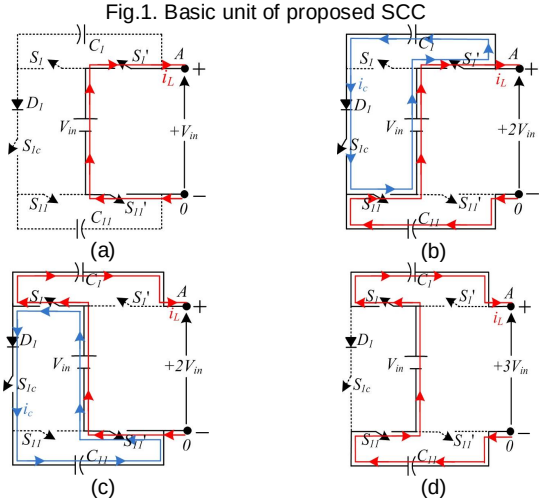

Fig.2. Equivalent circuit and current flow paths of proposed basic unit when V_{AO} is (a) $+V_{in}$, (b) $+2V_{in}$ (C_1 in charging state), (c) $+2V_{in}$ (C_{11} in charging state), (d) $+3V_{in}$ (both C_1 and C_{11} in discharging state)

TABLE I
SWITCH AND CAPACITOR STATES FOR BASIC UNIT

V_{AO}	Switches						Capacitors	
	S_1	S_1'	S_{11}	S_{11}'	S_{1c}	D_1	C_1	C_{11}
$+V_{in}$	0	1	0	1	0	0	NC	NC
$+2V_{in}$	0	1	1	0	1	1	C	D
$+2V_{in}$	1	0	0	1	1	1	D	C
$+3V_{in}$	1	0	1	0	0	0	D	D

$+2V_{in}$ output voltage level can be achieved by connecting one of the capacitors in series with V_{in}. Fig. 2(b) shows the equivalent circuit and current flow paths when C_{11} is in series with V_{in} by turning on S_1' and S_{11}. Hence, C_{11} is in discharging state as indicated by "D" in Table 1 and the output voltage is equal to the summation of the voltages of C_{11} and V_{in} which is approximately equal to $+2V_{in}$. At the same instant, by turning on S_{1c} in CH1, C_1 can be connected in parallel with V_{in}. Hence C_1 stores energy from V_{in} and is in charging state as depicted by "C" in Table 1.

Similarly, $+2V_{in}$ output voltage level can be produced across the output terminals by maintaining C_1 and C_{11} in discharging and charging state respectively as shown in Fig. 2(c). For discharging C_1, the switches S_1 and S_{11}' are maintained at on state whereas C_{11} can be maintained in the charging state by turning on S_{1c} in CH1 as shown in Table I. It is assumed that the magnitude of charging currents for both C_1 and C_{11} are equal and the charging current path (blue line) are shown in Fig. 2(b) and 2(c) respectively. The diode, D_1 is connected in series with S_{1c} in CH1 to avoid the unwanted discharging of C_1 or C_{11} into the supply voltage V_{in}.

When S_1 and S_{11} are in on state, C_1 and C_{11} are connected in series with V_{in} as depicted in Fig. 2(d). Hence, the capacitor voltages are added with V_{in} and appear across the output terminals. This voltage magnitude is approximately equal to $+3V_{in}$. In this circuit condition, both the capacitors are in discharging mode as shown in the Table I.

The following points can be concluded regarding the features of BU for the proposed SCC: (1) the BU can boost the output voltage three times of the input voltage V_{in}. Hence, the boosting factor of BU is 3; (2) the capacitors can be charged and discharged simultaneously. When C_1 is in charging state, at that instance C_{11} is in discharging state and *vice-versa*; (3) the switches in a capacitor legs are complementary to each other. Hence, the stress voltage across switches in L1 or L11 are equal to the capacitor voltage i.e. nearly V_{in}; (4) The voltage stress across the charging leg CH1 is equal to V_{in}. Hence, the total standing voltage of the BU is equal to $5V_{in}$.

III. GENERAL STRUCTURE OF PROPOSED SCC

In this section, the general structure of the proposed SCC is described. Fig. 3(a) shows the proposed SCC when two capacitor legs L2 and L22 and a charging leg CH2 are connected with the BU of proposed SCC which is shown in Fig. 1. This structure is called proposed SCC with n=2. Where n is the number of capacitor legs connected in one side of V_{in}. This structure is able to produce 9 positive output voltage levels. Fig. 3(b) shows the equivalent circuit and current flow path when the output voltage level is equal to $+3V_{in}$. In this circuit condition, the capacitors C_2 and C_{22} are in NC condition.

The capacitor C_2 or C_{22} can be charged to $3V_{in}$ when the output voltage level is equal to $+6V_{in}$. Fig. 3(c) shows the equivalent circuit and current flow paths when C_2 of L_2 is in charging state whereas C_{22} of L22 is in discharging state.

Similarly, Fig. 3(d) depicts the equivalent circuit and current flow paths when C_2 and C_{22} are in discharging and in charging state respectively. It can be noted that during $+6V_{in}$ output voltage level, C_1 and C_{11} of BU along with V_{in} pump their stored energy into output (V_{AO}) as well as charging either C_2 or C_{22}.

$+8V_{in}$ output voltage level is generated by adding V_{in}, any one capacitor voltage from BU and the capacitor voltages of L2 and L22. In this voltage level, any one of the capacitors from BU can be maintained in charging state as the BU circuit contributes $2V_{in}$ voltage to the output. Fig. 3(e) shows the equivalent circuit and current flow paths when the output voltage level is equal to $+8V_{in}$ and the capacitor C_1 is in charging state. In this circuit condition, the capacitors C_{11}, C_2, C_{22} are in discharging state. When all the capacitors are in discharging state, the output voltage is the summation of all the capacitor voltages and V_{in} which is equal to $+9V_{in}$. The equivalent circuit and current flow paths for the output voltage $+9V_{in}$ are shown in Fig. 3 (f).

The general structure of proposed SCC is shown in Fig. 4. It comprises of $2n$ number of capacitor legs and n number of

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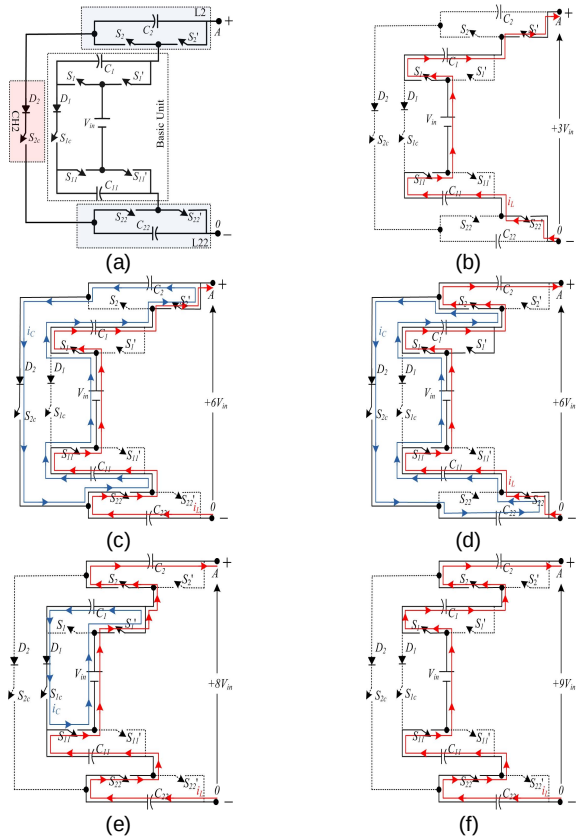

Fig.3. (a) Proposed SCC for *n=2*; equivalent circuit and current flow paths when V_{AO} is (b) $+3V_{in}$, (c) $+6V_{in}$ and C_2 is in charging state, (d) $+6V_{in}$ and C_{22} is in charging state, (e) $+8V_{in}$, (f) $+9V_{in}$

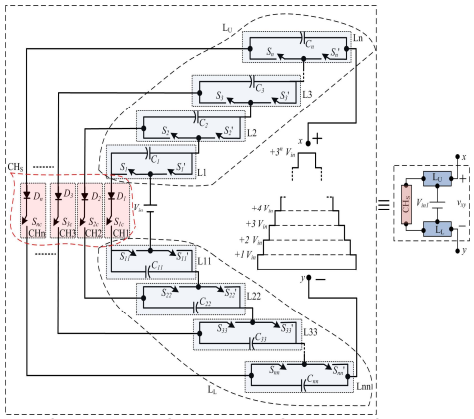

Fig.4. General structure of proposed SCC

charging legs. The capacitor legs L1, L2, L3,.....,Ln are connected with the positive terminal of V_{in} whereas the capacitor legs L11, L22, L33,.....,Lnn are connected with the negative terminal of V_{in}. The *n* number of charging legs CH1, CH2, CH3,.....,CHn are used to connect the capacitor legs in series as shown in Fig. 4. Further, a simplified equivalent structure of proposed SCC is shown in Fig. 4. The capacitor legs L1 to Ln are together represented by L_U whereas the capacitor legs L11 to Lnn are together represented by L_L. Similarly, the charging legs CH1 to CHn are together depicted by CHs. The capacitors associated with the capacitor legs in both the sides of V_{in} can be charged in trinary asymmetric pattern and the voltages of the capacitors can be expressed by (1).

$$V_{C_i} = V_{C_{ii}} = 3^{i-1}V_{in} \qquad \text{for } i = 1, 2, \ldots\ldots, n \tag{1}$$

With these capacitor voltages, the proposed SCC is able to produce 3^n number of positive voltage levels across its output terminals *x* and *y*. The on state switches in the legs and the capacitor states in the capacitors legs corresponding to the different output voltage levels of proposed SCC are tabulated in Table II. It should be noted that the proposed SCC is unable to charge the upper leg capacitor and the corresponding lower leg capacitor simultaneously as shown in Table II. However, as *n* is enhanced, the possibility of charging the capacitors increases significantly in a half cycle of the SCC output voltage. For an example, for *n*=1, the charging possibility for C_1 or C_{11} is one (at $+2V_{in}$ output voltage level). For *n*=2, C_1 or C_2 can be charged at $+2V_{in}$, $+5V_{in}$($3V_{in}+2V_{in}$) and $+8V_{in}$ ($3V_{in}+3V_{in}+2V_{in}$) output voltage levels. Hence, the possibility of charging for C_1 or C_{11} increases to three. Table III presents the number of charging possibility of different capacitors in the generalized proposed SCC with respect to *n*. In addition, the possibility of capacitor charging as well as capacitor voltage balancing of proposed SCC can be enhanced when a number of SCC circuits are connected together to form a inverter structure which is discussed in the next section.

IV. Comparison of Proposed SCC with other SCC Structures

In this section, the proposed SCC is compared with the SCC structures presented in **[18-19,21-23,24].** Table IV shows the comparison for number of required switches ($N_{sw(scc)}$), diodes ($N_{d(scc)}$) and capacitors ($N_{cap(scc)}$), per unit *TSV* ($TSV_{pu(scc)}$), the per unit maximum switch stress voltage ($V_{smpu(scc)}$), the maximum number of switches in the conducting path ($N_{p(scc)}$) for two values of output voltage level, $N_{L(scc)}$ for the proposed SCC and the suggested SCCs. The $TSV_{pu(scc)}$ and $V_{smpu(scc)}$ can be defined by (2). Where $V_{xy(max)}$ is the maximum output voltage magnitude produced by the SCCs.

$$TSV_{pu(scc)} = \frac{TSV}{V_{xy(\max)}};\ V_{smpu(scc)} = \frac{V_{sm}}{V_{xy(\max)}} \tag{2}$$

As Table IV indicates that for producing 9 output voltage levels, the proposed SCC requires significantly lower number of switches, capacitors, diodes as compared to the SCCs presented in **[18-19]** and **[24]**. Further, the SCC presented in **[21]** requires more number of diodes and capacitors for producing 9 output voltage levels as compared to proposed SCC. For generating 27 level output voltage by SCCs presented in **[18-19]** and **[21]**, and 24 level output voltage by the SCC presented in **[24]**, the requirement of components is significantly higher as compared to the proposed SCC. This comparison signifies that the proposed SCC requires lower components for realizing a specific output voltage levels as compared to **[19, 21, 24]**. However, the proposed SCCs in **[19]** and **[21]** cannot produce capacitor voltage more than the input voltage, the $TSV_{pu(scc)}$ and $V_{smpu(scc)}$ of these SCCs are lower as compared to proposed SCC. The SCC presented in **[24]** sustains higher $TSV_{pu(scc)}$ and $V_{smpu(scc)}$ as compared to proposed SCC.

TABLE II
SWITCH AND CAPACITOR STATES FOR PROPOSED SCC

Output Voltage (V_{xy})	On switches in capacitor legs and charging legs			Capacitor states	
	L1 L2 L3.....Ln	L11 L22 L33....Lnn	CH1 CH2 CH3 ..... CHn	C_1 C_2 C_3.....C_n	C_{11} C_{22} C_{33}..... C_{nn}
$+V_{in}$	S_1' S_2' S_3'....S_n'	S_{11}' S_{22}' S_{33}'...S_{nn}'	- - - ..... -	NC NC NC.....NC	NC NC NC.....NC
$+2V_{in}$	S_1' S_2' S_3'....S_n'	S_{11} S_{22}' S_{33}'...S_{nn}'	S_{1c} - - ..... -	C NC NC.....NC	D NC NC.....NC
	S_1 S_2' S_3'....S_n'	S_{11}' S_{22}' S_{33}'...S_{nn}'	S_{1c} - - ..... -	D NC NC.....NC	C NC NC.....NC
$+3V_{in}$	S_1 S_2' S_3'....S_n'	S_{11} S_{22}' S_{33}'...S_{nn}'	- - - ..... -	D NC NC.....NC	D NC NC.....NC
$+4V_{in}$	S_1' S_2' S_3'....S_n'	S_{11}' S_{22} S_{33}'...S_{nn}'	- - - ..... -	NC NC NC.....NC	NC D NC.....NC
	S_1' S_2 S_3'....S_n'	S_{11}' S_{22}' S_{33}'...S_{nn}'	- - - ..... -	NC D NC..... NC	NC NC NC.....NC
$+5V_{in}$	S_1' S_2' S_3'....S_n'	S_{11} S_{22} S_{33}'...S_{nn}'	S_{1c} - - ..... -	C NC NC.....NC	D D NC.....NC
	S_1 S_2' S_3'....S_n'	S_{11}' S_{22} S_{33}'...S_{nn}'	S_{1c} - - ..... -	D NC NC.....NC	C D NC.....NC
	S_1 S_2 S_3'....S_n'	S_{11}' S_{22}' S_{33}'...S_{nn}'	S_{1c} - - ..... -	D D NC.....NC	C NC NC.....NC
	S_1' S_2 S_3'....S_n'	S_{11} S_{22}' S_{33}'...S_{nn}'	S_{1c} - - ..... -	C D NC.....NC	D NC NC.....NC
$+6V_{in}$	S_1 S_2' S_3'....S_n'	S_{11} S_{22} S_{33}'...S_{nn}'	- S_{2c} - ..... -	D NC NC.....NC	D D NC.....NC
	S_1 S_2 S_3'....S_n'	S_{11} S_{22}' S_{33}'...S_{nn}'	- S_{2c} - ..... -	D D NC.....NC	D NC NC.....NC
$+7V_{in}$	S_1' S_2 S_3'....S_n'	S_{11}' S_{22} S_{33}'...S_{nn}'	- - - ..... -	NC D NC.....NC	NC D NC.....NC
$+8V_{in}$	S_1' S_2 S_3'....S_n'	S_{11} S_{22} S_{33}'...S_{nn}'	S_{1c} - - ..... -	C D NC.....NC	D D NC.....NC
	S_1 S_2 S_3'....S_n'	S_{11}' S_{22} S_{33}'...S_{nn}'	S_{1c} - - ..... -	D D NC.....NC	C D NC.....NC
$+9V_{in}$	S_1 S_2 S_3'....S_n'	S_{11} S_{22} S_{33}'...S_{nn}'	- - - ..... -	D D NC.....NC	D D NC.....NC
.....	.....			.....	
$+3^nV_{in}$	S_1 S_2 S_3....S_n	S_{11} S_{22} S_{33}....S_{nn}	- - - ..... -	D D D .....D	D D D .....D

TABLE III
POSSIBILITY OF CHARGING OF CAPACITORS IN HALF CYCLE OF SCC OUTPUT VOLTAGE CYCLE

Capacitors	**Possibility of charging**
C_1 or C_{11}	3^{n-1}
C_2 or C_{22}	3^{n-2}
C_3 or C_{33}	3^{n-3}
.....	.....
C_{n-1} or $C_{(n-1)(n-1)}$	3^1
C_n or C_{nn}	3^0

TABLE IV
COMPARISON OF PROPOSED SCC WITH OTHER SCC CIRCUITS

Topology Presented in	$N_{L(scc)}$	$N_{sw(scc)}$	$N_{d(scc)}$	$N_{cap(scc)}$	$N_{p(scc)}$	$V_{xy(\max)}$	$TSV_{pu(scc)}$	$V_{smpu(scc)}$
[18]	9	24	-	8	8	$9V_{in}$	2.67	0.11
	27	78	-	26	26	$27V_{in}$	2.88	0.037
[19]	9	16	8	8	8	$9V_{in}$	1.78	0.11
	27	52	26	26	26	$27V_{in}$	1.92	0.037
[21]	9	9	16	8	8	$9V_{in}$	1	0.11
	27	27	52	26	26	$27V_{in}$	1	0.037
[22-23]	8	8	3	3	3	$8V_{in}$	2.62	0.5
	32	14	5	5	5	$32V_{in}$	2.9	0.5
[24]	9	24	-	5	8	$9V_{in}$	6	0.33
	24	42	-	9	10	$24V_{in}$	3.67	0.25
Proposed Topology	9	10	2	4	4	$9V_{in}$	2.22	0.33
	27	15	3	6	6	$27V_{in}$	2.4	0.33

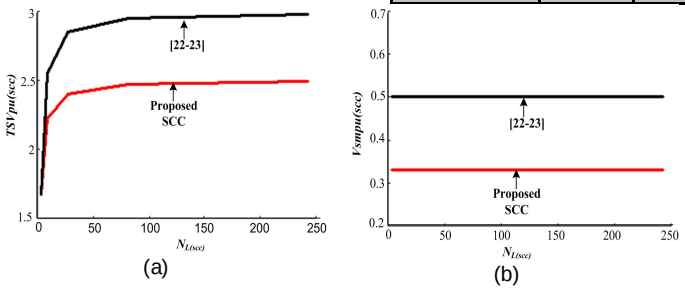

Fig.5 Comparison of proposed SCC with the SCCs presented in [22] and [23] in respect of (a) per unit *TSV* and (b) per unit maximum switch stress voltage.

As seen from the Table IV, the proposed SCC requires higher number of switches and capacitors, and lower number of diodes for generating a $N_{L(scc)}$ as compared to SCCs proposed in **[22-23]**. However, the proposed SCC provides significantly lower $TSV_{pu(scc)}$ and $V_{smpu(scc)}$ as compared to **[22-23]**. In Table IV, $TSV_{pu(scc)}$ and $V_{smpu(scc)}$ for proposed SCC producing 9 output voltage levels, are 2.22 and 0.33 respectively, whereas the same parameters for the SCC presented in **[22-23]** which generates 8 output voltage level, are 2.62 and 0.5 respectively. Further, the variation of $TSV_{pu(scc)}$ and $V_{smpu(scc)}$ with respect to $N_{L(scc)}$ are shown in Fig. 5(a) and 5(b) respectively.

V. PROPOSED SCMLI STRUCTURE

In this section, Cross Switched MLI (CS-MLI) **[9]** with the proposed SCC is developed and discussed. Fig. 6. shows the CS-MLI with *m* number of proposed SCCs. Output voltages of SCCs are v_{o1}, v_{o2}, v_{o3},.....,v_{om} . Table V presents switching

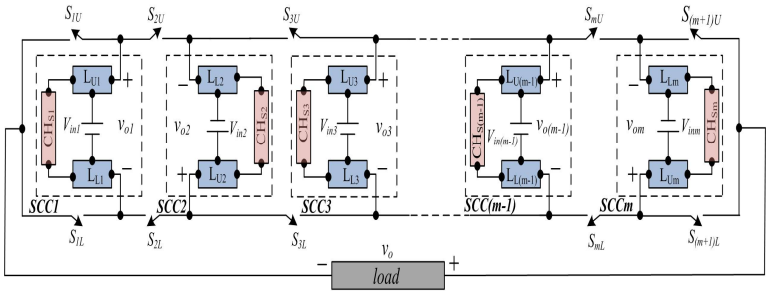

Fig. 6. Proposed cross-switched SCMLI structure

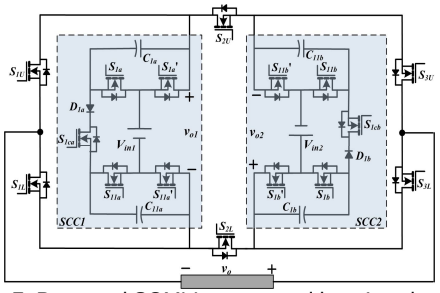

Fig. 7. Proposed SCMLI structure with *n*=1 and *m*=2

states to generate the output voltage (v_o) of CS-MLI in terms of SCC voltages. The maximum value of v_o is the summation of all the SCC voltages.

The required number of switches (N_{sw}), gate drivers (N_{dr}), capacitors (N_{cap}), diodes (N_d) and dc sources (N_{dc}) in terms of *m* and *n* for the proposed MLI can be expressed by (3) to (6). The proposed MLI does not possess the capability to generate the output voltage levels equal to the summation of even or odd position SCC unit output voltages. For example, the proposed topology cannot produce output voltage equal to (v_{o1}+v_{o3}+v_{o5}) or (v_{o2}+v_{o4}+v_{o6}). To avoid this, the proposed MLI is analyzed for symmetric and asymmetric dc source configurations.

TABLE V
DIFFERENT OUTPUT VOLTAGE LEVELS OF SCMLI IN TERMS OF SCC UNIT VOLTAGES

v_o	on switches
0	S_{1U} , S_{2U} , S_{3U} ,....., S_{mU} , $S_{(m+1)U}$
	S_{1L} , S_{2L} , S_{3L} ,....., S_{mL} , $S_{(m+1)L}$
v_{o1}	S_{1L} , S_{2U} , S_{3U} ,....., S_{mU} , $S_{(m+1)U}$
v_{o2}	S_{1U} , S_{2U} , S_{3L} ,....., S_{mL} , $S_{(m+1)L}$
v_{o3}	S_{1L} , S_{2L} , S_{3L} , S_{4U} ,....., S_{mU} , $S_{(m+1)U}$
$v_{o1}+v_{o2}$	S_{1L} , S_{2U} , S_{3L} ,....., S_{mL} , $S_{(m+1)L}$
$v_{o1}+v_{o2}+v_{o3}$	S_{1L} , S_{2U} , S_{3L} , S_{4U} ,....., S_{mU} , $S_{(m+1)U}$
.....	.....
$v_{o1}+v_{o2}+v_{o3}+...+v_{om}$	S_{1L} , S_{2U} , S_{3L} , S_{4U} ,....., S_{mU} , $S_{(m+1)L}$

$$N_{sw} = N_{dr} = (5n+2)m+2 \quad (3)$$

$$N_{cap} = 2nm \quad (4)$$

$$N_d = nm \quad (5)$$

$$N_{dc} = m \quad (6)$$

$$V_{inj} = V_{dc} \text{ for } j = 1,2,3,.....,m \quad (7)$$

$$N_L = (2m3^n)+1 \quad (8)$$

$$v_{o\max} = m3^n V_{dc} \quad (9)$$

$$TSV = m[\frac{13(3^n)-5}{2}]V_{dc} \quad (10)$$

A. Symmetric configuration

In symmetric configuration, all the dc sources for SCCs have same voltage magnitudes as shown in (7). With this configuration the generated output voltage levels (N_L), the maximum output voltage magnitude (v_{omax}) and *TSV* of the inverter can be expressed by (8) to (10). With *n=1* and *m=2*, the proposed MLI can produce 13 output voltage levels. Fig. 7 shows the proposed SCMLI with *n=1* and *m=2*. Table VI presents the switching and capacitor states of the proposed 13 level SCMLI. The switching states are selected in such a manner that the minimum switching transition will occur. Further, in every output voltage level except maximum voltage levels, at least one of the capacitors will be either in charging (C) or in not-connected (NC) state condition.

TABLE VI
SWITCHING AND CAPACITOR STATES OF THE PROPOSED SYMMETRICAL 13 LEVEL SCMLI

$\frac{v_o}{V_{dc}}$	on switches	C_{1a}	C_{11a}	C_{1b}	C_{11b}
+6	$S_{1L}, S_{11a}, S_{1a}, S_{2U}, S_{11b}, S_{1b}, S_{3L}$	D	D	D	D
+5	$S_{1L}, S_{11a}', S_{1a}, S_{2U}, S_{11b}, S_{1b}, S_{3L}, S_{1ca}$	D	C	D	D
+4	$S_{1L}, S_{11a}, S_{1a}', S_{2U}, S_{11b}', S_{1b}, S_{3L}, S_{1ca}, S_{1cb}$	C	D	C	D
+3	$S_{1L}, S_{11a}', S_{1a}, S_{2U}, S_{11b}', S_{1b}', S_{3L}$	D	NC	NC	NC
+2	$S_{1U}, S_{2U}, S_{11b}, S_{1b}', S_{3L}, S_{1cb}$	NC	NC	D	C
+1	$S_{1U}, S_{2U}, S_{11b}', S_{1b}', S_{3L}, S_{11a}', S_{1a}, S_{1ca}$	NC	C	NC	NC
0	$S_{1L}, S_{2L}, S_{3L}, S_{1a}', S_{11a}, S_{1ca}, S_{11b}', S_{1b}, S_{1cb}$	C	NC	C	NC
−1	$S_{1L}, S_{2L}, S_{1b}', S_{11b}', S_{3U}, S_{1a}, S_{11a}', S_{1ca}$	NC	C	NC	NC
−2	$S_{1L}, S_{2L}, S_{1b}', S_{11b}, S_{3U}, S_{1cb}$	NC	NC	D	C
−3	$S_{1U}, S_{1a}, S_{11a}', S_{2L}, S_{1b}', S_{11b}', S_{3U}$	D	NC	NC	NC
−4	$S_{1U}, S_{1a}', S_{11a}, S_{2L}, S_{1b}, S_{11b}', S_{3U}, S_{1ca}, S_{1cb}$	C	D	C	D
−5	$S_{1U}, S_{1a}, S_{11a}, S_{2L}, S_{1b}', S_{11b}, S_{3U}, S_{1cb}$	D	D	D	C
−6	$S_{1U}, S_{1a}, S_{11a}, S_{2L}, S_{1b}, S_{11b}, S_{3U}$	D	D	D	D

B. Asymmetric configuration

For generating higher voltage levels using minimum number of switches, asymmetric configuration has been proposed. In this configuration, the dc sources for proposed MLI are selected as (11) and (12). For *n=1*, the dc sources for SCC 1, SCC 2,....,SCC *m* are V_{dc}, $4V_{dc}$, $12V_{dc}$, $36V_{dc}$,...,$3^{(m-2)}4V_{dc}$ respectively. With *n=1* and *m=3*, the MLI can produce 103 voltage levels utilizing 23 switches and 3 sources. N_L, v_{omax} of the MLI with this configuration can be expressed by (13) to (14).

$$V_{in1} = V_{dc} \quad (11)$$

$$V_{inj} = 3^{j-2}\left(3^n+1\right)V_{dc} \text{ ; for } j = 2,3,.....,m \quad (12)$$

$$N_L = 2[3^n\{1+\frac{1}{2}\{(3^n+1)(3^{m-1}-1)\}\}]+1 \text{ ; for } m \geq 2 \quad (13)$$

$$v_{o\max} = [3^n\{1+\frac{1}{2}\{(3^n+1)(3^{m-1}-1)\}\}]V_{dc} \text{ ; for } m \geq 2 \quad (14)$$

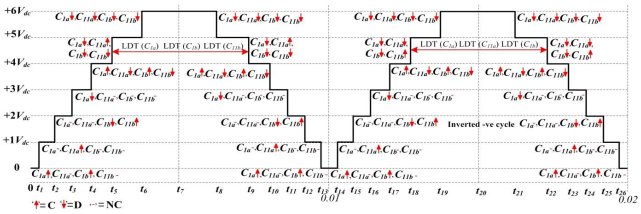

Fig. 8. 13 level output voltage waveform (inverted negative cycle) with LDT for different capacitors

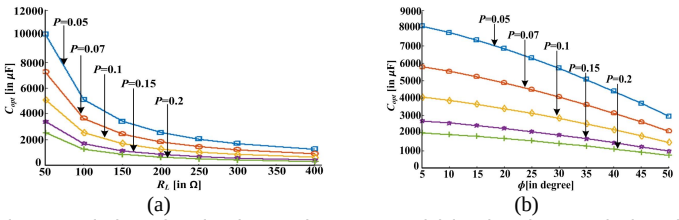

Fig. 9. Variation of optimal capacitance w.r.t. (a) load resistance (R_L) and (b) phase angle (ϕ) for different percentage of capacitor voltage ripples (p)

VI. Selection Procedure of Capacitance for Switched Capacitors

This section presents the selection procedure of capacitance for the switched capacitors (SCs) used in 13 level proposed SCMLI. For evaluating the capacitance value, the longest discharging time(LDT) for each capacitor over a fundamental output voltage cycle is to be calculated **[18, 22, 26]**. The 13 level output voltage with inverted negative cycle is depicted in Fig. 8. Based on the switching state as presented in Table IV, the LDT for different capacitors are shown in Fig. 8 (in red colour). During LDT, the capacitor discharges maximum amount of charge. The amount of discharging charge depends on the load current and LDT duration. The amount of discharging charge for the utilized SCs in 13 level SCMLI can be expressed by (15).

$$Q_{C_{1a}} = Q_{C_{11a}} = Q_{C_{1b}} = Q_{C_{11b}} = 2\times \int_{t5}^{T/4} i_o(t)\, dt = 2\times \int_{t18}^{3T/4} i_o(t)\, dt \tag{15}$$

Considering the maximum allowable voltage ripple is p percentage of steady state capacitor voltage, the value of optimal capacitance for the SCs can be expressed by (16).

$$C_{opt} \geq \frac{Q_{C_{1a}} \text{ or } Q_{C_{11a}} \text{ or } Q_{C_{1b}} \text{ or } Q_{C_{11b}}}{p\times V_{dc}} \tag{16}$$

For resistive load (R_L) condition, the load current during the LDT can be expressed by (17).

$$\begin{aligned} i_o(t) &= \frac{5V_{dc}}{R_L} \quad \text{for} \quad t_5 \leq t \leq t_6 \\ &= \frac{6V_{dc}}{R_L} \quad \text{for} \quad t_6 \leq t \leq \frac{T}{4} \end{aligned} \tag{17}$$

Considering fundamental switching frequency scheme, the time t_5 and t_6 can be evaluated by (18).

$$\begin{aligned} t_5 &= \frac{Sin^{-1}(9/12)}{2\pi f} \text{ sec} \\ t_6 &= \frac{Sin^{-1}(11/12)}{2\pi f} \text{ sec} \end{aligned} \tag{18}$$

By using the equations (15), (16), (17) and (18), the optimal value of capacitance for resistive load condition can be expressed by (19).

$$C_{opt} \geq \frac{8}{2\pi \times f \times R_L \times p} \tag{19}$$

From (19), it can be noted that the optimum capacitor value is inversely proportional to the load resistance, output frequency and the percentage of voltage ripple. Considering 50Hz as the fundamental output frequency, the variation of optimal capacitance for different percentage of capacitor voltage ripple is shown in Fig. 9(a). As the capacitor voltage ripple increases, the required capacitance value decreases at a constant load resistance.

For resistive-inductive (R-L) load condition, the load current during the LDT can be expressed by a sinusoidal function with a maximum current amplitude of I_{omax} lagging the fundamental output voltage by ϕ as shown in (20).

$$i_o(t) = I_{o\max} Sin(2\pi f - \phi) \tag{20}$$

The optimum capacitance value for R-L load condition can be achieved by solving the equation (16) using the equations (15), (18) and (20). The optimum value of capacitance can be represented by (21).

$$C_{opt} \geq \frac{I_{o\max}}{2\pi \times f \times p \times V_{dc}} [Cos(0.8481 - \phi) - Sin\phi] \tag{21}$$

The variation of optimal capacitance value for different ϕ angles and percentage of voltage ripple, p is presented in Fig. 9(b) for I_{omax}=3A, V_{dc}=30V and f=50Hz. It can be observed that as the ϕ increases the value of required capacitance decreases for a constant voltage ripple. Similarly, as the voltage ripple increases, the required capacitance value decreases at a constant ϕ.

VII. Comparison Study

In this section, the proposed SCMLI has been compared with the SCMLIs presented in **[20, 22-23, 25-26]** with respect to different points of view such as required components, *TSV* of the structures. Further, the topologies are compared based on a cost function (*CF*) [**26**] as shown in (22) for a fair comparison.

$$CF = \left(N_{sw} + N_{dr} + N_d + N_{cap} + \beta TSV_{pu}\right) \times N_{dc} \tag{22}$$

Where β presents the weightage of the *TSV*. The comparison study is presented in the following sub-sections:

A. Comparison study based on symmetric dc sources

Table VII presents the comparison study with symmetric dc sources. It can be noted that for N_L=13, the proposed topology uses 2 dc sources and 16 switches (n=1 and m=2) whereas the topology presented in **[20]** requires 3 dc sources and 18 switches. The topology presented here produces 37 output voltage levels using less number of dc sources, switches, drivers and diodes as compared to the 33 level topology in **[22]**. Further, the topology in **[22]** provides significantly higher cost function/level (CF/N_L) for both the values of β as compared to proposed topology. As compared to **[25-26]**, the proposed topology requires higher component count and *TSV* at lower N_L, however, as N_L enhances, the component count as well as CF/N_L decrease significantly.

B. Comparison study based on asymmetric dc sources

Table VIII presents the required component counts, *TSV* and CF/N_L for all the topologies for asymmetric dc sources. Based

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TABLE VII
COMPARISON OF PROPOSED SCMLI WITH OTHER SCMLIS WITH SYMMETRIC DC SOURCE CONFIGURATION

SCMLI presented in	N_L	N_{dc}	N_{sw}	N_{dri}	N_{dio}	N_{cap}	TSV_{pu}	CF/N_L	
								$\beta=0.5$	$\beta=1.5$
[20]	13	3	18	18	3	3	5	10.26	11.42
[22]	17 (n=1,m=2)	4	20	20	4	4	5	11.88	13.05
	33 (n=2, m=2)	4	32	32	8	8	6	10.06	10.78
[25]	13	2	14	14	4	4	5.3	5.94	6.76
	37	2	38	38	16	16	6.11	6	6.33
[26]	17	2	18	14	2	4	5	4.76	5.35
	33	4	34	26	4	8	4.5	9	9.54
Proposed Topology	13 (n=1, m=2)	2	16	16	2	4	5.6	6.27	7.13
	37 (n=2, m=2)	2	26	26	4	8	6.22	3.62	3.96

TABLE VIII
COMPARISON OF PROPOSED SCMLI WITH OTHER SCMLIS WITH ASYMMETRIC DC SOURCE CONFIGURATION

SCMLI presented in	N_L	N_{dc}	N_{sw}	N_{dri}	N_{dio}	N_{cap}	TSV_{pu}	CF/N_L	
								$\beta=0.5$	$\beta=1.5$
[22]	49 (n=2, m=1)	2	16	16	4	4	6.25	1.76	2.01
	289 (n=1, m=2)	4	20	20	4	4	5.5	0.702	0.78
[23]	17	2	10	10	2	2	5.5	3.14	3.79
	137	4	18	18	4	4	6	1.37	1.55
[25]	31	2	14	14	4	4	5.33	2.49	2.83
	199	2	38	38	16	16	5.77	1.114	1.17
[26]	49	2	18	14	2	4	6	1.67	1.91
	249	3	26	20	3	6	6.40	0.701	0.778
Proposed Topology	31 (n=1, m=2)	2	16	16	2	4	5.67	2.63	3.00
	199 (n=m=2)	2	26	26	4	8	6.22	0.674	0.736

on this Table, it is observed that the proposed structure with asymmetric dc sources is not significantly beneficial as compared to suggested topologies for producing lower output voltage levels. However, for large voltage level generation, the proposed topology requires lower dc sources as compared to others. Further, the proposed topology provides lower CF/N_L as compared to the suggested topologies at high N_L for both β values. The asymmetric structure of topology in **[25]** requires significantly high component counts to realize high N_L as compared to proposed topology.

VIII. EXPERIMENTAL STUDIES

This section presents the experimental studies for 13 level (n=1, m=1) and 37 level (n=m=2) proposed SCMLI structures. A laboratory prototype of the proposed SCMLI with n=1 and m=2 has been developed first as shown in Fig. 10. After that the same structure has been extended for n=2 and m=2. MOSFET has been selected as the switching devices for the practical set-up. As in the structure, the switches S_{2U} and S_{2L} have to withstand the highest voltage stress, IRF 840 (500V, 8A) has been chosen as the switching device for them. The rest of the switches in the structure are IRF640 (200V, 18A). Fundamental frequency switching scheme is employed. The different switching pulses are produced by dSpace controller (DS-1104). IR2110 IC is chosen as the gate driver IC for driving the switches.

A. Experimental results for 13 level proposed SCMLI

This sub-section presents the experimental results for 13 level proposed symmetric SCMLI structure. The magnitude of the dc voltage sources are chosen as 30V each. The capacitance value for the SCs are equal and selected as 2500μF each. This capacitance value has been calculated based on 15% voltage ripple of steady state capacitor voltage (as shown in p=0.15 in Fig. 9(b) with ϕ=16.8^0 lagging load condition and peak load current is considered as 3A).

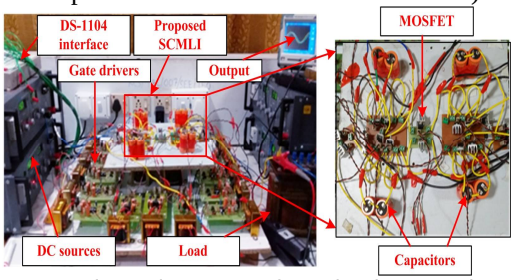

Fig. 10. Experimental test set-up for 13 level proposed SCMLI

Fig. 11(a) shows the experimental waveforms for output voltage $v_o(t)$ and load current $i_L(t)$ when the inverter is loaded with R-L load (R=52Ω and L=50mH). It can be observed that the output voltage waveform consists of 13 voltage levels. From the FFT analysis of output voltage, it is found that the peak magnitude of fundamental voltage and total harmonic distortion (THD) of output voltage are 163.1V and 7.57% respectively. Similarly from the FFT analysis of load current, the peak magnitude of fundamental current and THD of load current are found as 3.01A and 3.26% respectively. Under this load condition, the output power of the inverter is evaluated as 226W whereas the total losses of the inverter is evaluated as 19.25W (conduction loss=13.5W, capacitor ripple loss=6.25W, switching loss=10mW). The experimental efficiency of the inverter is 92.1%. Under the same load condition, the steady state capacitor voltages and their voltage ripples are depicted in Fig. 11(b) and 11(c) respectively. It can be observed that voltage for C_{1a}, C_{11a}, C_{1b} and C_{11b} are 26.5V,

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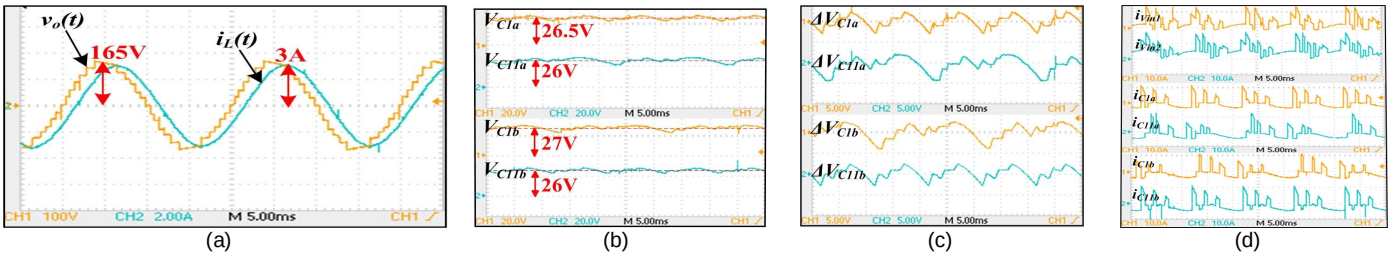


(a) (b) (c) (d)

Fig.11. Experimental waveforms for (a) steady state 13 level load voltage and load current (100V/div and 2A/div), (b) capacitor voltages (20V/div), (c) capacitor voltage ripples(5V/div) and (d) source currents (10A/div) and capacitor currents (10A/div) for *R-L* (*R*=52Ω and *L*=50mH) load condition

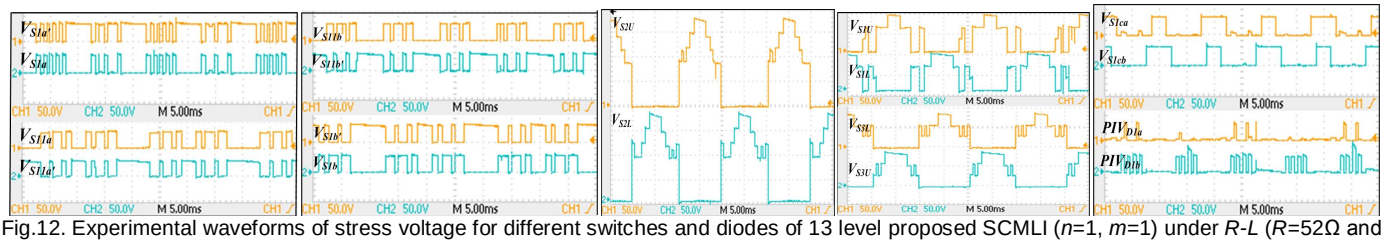
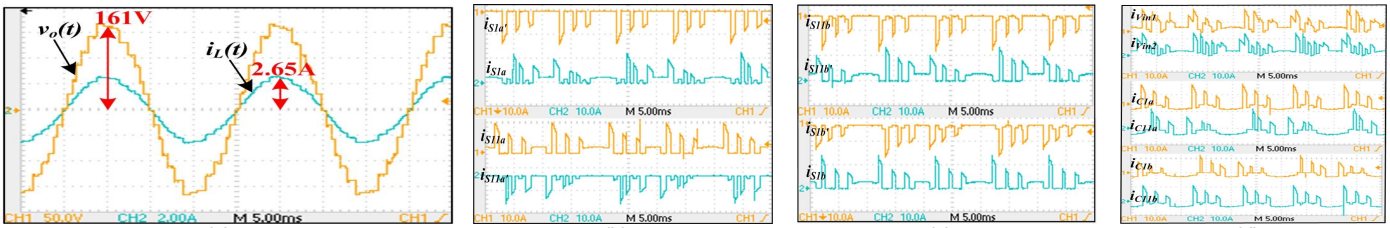
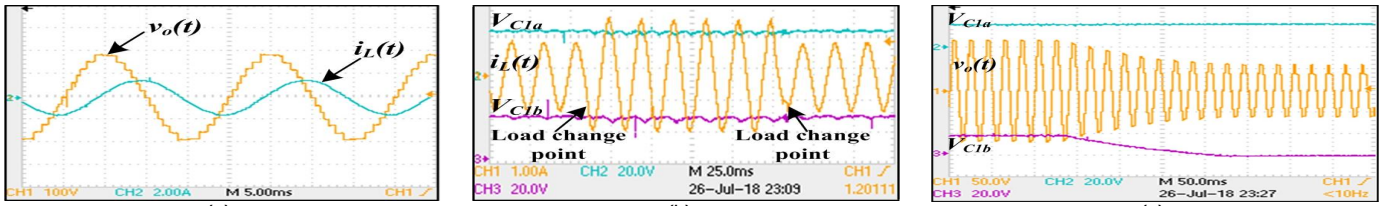


Fig.12. Experimental waveforms of stress voltage for different switches and diodes of 13 level proposed SCMLI (*n*=1, *m*=1) under *R-L* (*R*=52Ω and *L*=50mH) load condition



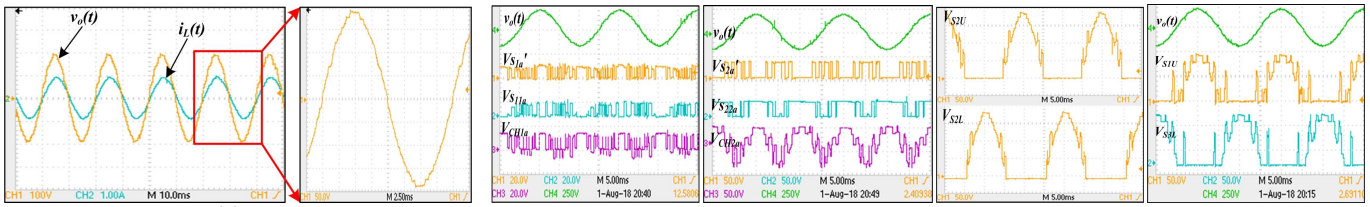
(a) (b) (c) (d)

Fig.13. Experimental waveforms for (a) steady state 13 level output voltage and load current (50V/div and 2A/div), (b)current through the SC cell switches in SCC a (10A/div), (c) current through the SC cell switches in SCC b (10A/div), and (d) source currents (10A/div) and capacitor currents (10A/div) for *R* (*R*=60Ω) load condition



(a) (b) (c)

Fig.14. Experimental waveforms for (a) steady state 13 level load voltage and load current (100V/div and 2A/div) for *L* (*L*=275mH) load,(b) load current (1A/div) and capacitor voltages (20V/div) under sudden load change condition, (c) load voltage (50V/div) and capacitor voltages(20V/div) when one of the sources (V_{in2}) is suddenly blocked out



(a) (b)

Fig. 15. Experimental waveforms for (a) steady state 37 level load voltage with load current (100V/div and 1A/div), (b) load voltage with stress voltage across S_{1a}', S_{11a} and stress voltage across charging leg 1 (CH1) (20V/div); load voltage with stress voltage across S_{2a}', S_{22a} and stress voltage across charging leg 2 (CH2) (50V/div); stress voltage across S_{2U} and S_{2L} (50V/div), load voltage with stress voltage across S_{1U} and S_{3L} (50V/div)

26V, 27V and 26V respectively. The voltage ripples of the capacitors are within 5.5V. Fig. 11(d) presents the source and capacitor currents for this same load condition.

Fig. 12 shows the stress (block) voltage across the different switches of 13 level inverter structure under *R-L* load condition. The maximum stress voltage for S_{1a}, S_{1a}', S_{11a}, S_{11a}', S_{1b}, S_{1b}', S_{11b} and S_{11b}' are equal and within 30V (as shown in left side of Fig. (12)). The maximum stress voltage for the switches S_{2U} and S_{2L} are equal and within 200V (as shown in middle of Fig. (12)). Further, the maximum stress voltage for

the switches S_{lU}, S_{1L}, S_{3U} and S_{3L} are equal and within 100V. Furthermore, the maximum stress voltage for the switches S_{1ca} and S_{1cb} are equal and within 30V. Similarly the peak inverse voltage (PIV) of the utilized diodes D_{1a} and D_{1b} in charging legs are equal and within 30V (as shown in right side of Fig. (12)).

After *R-L* load, the 13 level inverter structure has been tested for resistive load (*R*) of 60Ω with same magnitude (30V) of dc voltage sources and the same SCs (2500μF). The experimental output voltage and load current for this load condition are depicted in Fig. 13(a). It can be observed that the top level of the output voltage waveform is damaged and decaying with time due to the discharging state of all the SCs in this voltage level. As the load current is increased, this effect becomes more prominent.

Fig. 13(b) and 13(c) depict the current through the switches associated with the SC cells. From these figures, it can be observed that under resistive load condition, the current through the switches S_{1a}', S_{11a}', S_{11b} and S_{1b}' are passing through body diode and the current is only the charging current for the switched capacitors. Hence, the current through these switches can be expressed by (23).

$$i_{S1a'} = i_{S11a'} = i_{S11b} = i_{S1b'} = i_C(t) = C\frac{dv_c}{dt} \tag{23}$$

$$i_{S1a} = i_{S11a} = i_{S11b'} = i_{S1b} = i_L(t) + i_C(t) = i_L(t) + C\frac{dv_c}{dt} \tag{24}$$

Similarly, the rest of the SC cell switches carry the current which is the summation of load current and capacitor charging current. Hence, for the other SC cell switches, the current can be expressed by (24). However, the spike current for all the switches are due to the capacitor charging current. The magnitude of the spike current will be more if the capacitance of the switched capacitor are increased as well as if the rate of change of capacitor voltage increases. Further, as the power level of the inverter increases, the spike current through the switches becomes higher. With the load current of 3A and the capacitors of 2500µF, the spike current for the switches S_{1a}', S_{11a}', S_{11b} and S_{1b}' is around 10A whereas the spike current for the rest of the switches is around 13A. These current spikes can be reduced by selecting optimum capacitor values and increasing the voltage rise time of the capacitor voltages. Further, Fig. 13(d) shows the source and capacitor currents for this load condition.

In addition of *R-L* and *R* load conditions, the 13 level inverter structure has been successfully tested for the inductive (*L*) and sudden step change load conditions. Fig. 14(a) shows the output voltage and load current waveforms for *L*=275mH. It can be observed that the load current lags the output voltage by 90degree. Fig. 14(b) shows the load current and capacitor voltages for sudden step change in the load resistance. It can be observed that the load current and capacitor voltages are stable after sudden increment/decrement of load. Further, the performance of inverter has been tested when one of the dc source is suddenly blocked out. For this test, the supply voltages are selected as 20V each. From Fig. 14(c), it can be observed that after blocking out one of the supplies, the output voltage waveform consists of less number of voltage levels and the capacitors which were charged by the blocked supply previously discharge their stored energy and the voltage across the capacitors become zero.

B. Experimental results for 37 level proposed SCMLI

In this sub-section, the experimental results for 37 level proposed symmetrical SCMLI structure (*n*=*m*=2)are presented. The laboratory prototype has been implemented by incorporating the another two additional capacitor legs in each SCCs of 13 level SCMLI. The selected capacitors for the structures are 2500µF for C_{1a}, C_{11a}, C_{1b} and C_{11b} whereas 1880μF for C_{2a}, C_{22a}, C_{2b} and C_{22b}. The magnitude of supply voltages are selected as 15V each. With these dc supplies, the structure is able to produce a 37 level output voltage waveform of peak voltage level of 200V as shown in Fig. 15(a). Further, Fig. 15(a) shows the load current for *R-L* load condition (*R*=200Ω, *L*=50mH).

The stress voltage across different switches for the 37 level inverter structure are shown in Fig. 15(b). The stress voltage for the switches S_{1a}', S_{11a}, charging leg CH1a, S_{2a}', S_{22a} and charging leg CH2a are shown in left side of Fig. 15(b). It can be observed that the maximum stress voltage for S_{1a}', S_{11a}, charging leg CH1a are same and within 15V whereas the maximum stress voltage for the switches S_{2a}', S_{22a}, charging leg CH2a are same and within 40V. Similarly, the stress voltage across the switches S_{2U} and S_{2L} are equal and within 200V as shown in middle of Fig. 15(b). Furthermore, the stress voltage across the switches S_{1U} and S_{3L} are equal and within 100V as shown in the right side of Fig. 15(b).

IX. Conclusion

At first, a novel SCC structure has been proposed in this paper. The proposed SCC has the ability to produce boosted multistep dc voltages from an input dc source. The capacitors used in the SCC structure can be charged in trinary asymmetrical patter. Further, the SCC shows the lower *TSV* and lower maximum switch stress voltage as compared to other recently published SCC structures. After that a SCMLI structure has been developed and analyzed for symmetric and asymmetric dc source configurations. The SCMLI structure is able to produce a specific output voltage level with utilizing lower semiconductor devices, capacitors and sustaining lower *TSV* as compared to most of the suggested SCMLI structures. Further, the overall cost comparison of proposed SCMLI with other SCMLIs shows that the proposed structure is more cost effective as compared to most of the SCMLIs for symmetric dc source configuration and as compared to few of the suggested SCMLIs for asymmetric dc source configuration. The performance of proposed 13 level and 37 level symmetric SCMLI structures has been verified by conducting extensive experimental studies on laboratory prototypes. The proposed SCMLI is suitable for solar PV standalone applications such as water pumping systems, Uninterrupted Power Supply (UPS) applications, motor drive applications.

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